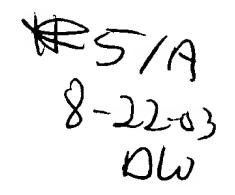


## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



**Applicant** 

: Bedichek, R.

Serial No.

: 09/417,332

Group Art Unit: 2183

Filed

: 10/13/1999

Examiner: Ellis, R.

For

: METHOD FOR INTEGRATION OF INTERPRETATION AND

TRANSLATION IN A MICROPROCESSOR

## **RESPONSE TO OFFICE ACTION**

RECEIVED

AUG 1 9 2003

Assistant Commissioner for Patents & Trademarks Washington, D.C. 20231

Technology Center 2100

Examiner: Ellis, R.

Group Art Unit: 2183

Sir:

In response to the Office Action mailed 5/13/03, please consider the following amendments and remarks.